SERIES II CNC
MILLING, DRILLING AND BORING MACHINE
(BOSS 6 AND 6.2 CONTROLS)
MAINTENANCE MANUAL

February 1982

Missing Sheets 2-1, 13-19, 13-20
I would VERY MUCH Like to thank
John Lafergola for compiling this book from individual Pictures.

Bridgeport® TEXTRON

Bridgeport Machines Division of Textron Inc.

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SECTION I
INTRODUCTION

1.1 PURPOSE

In this manual we provide the information necessary to maintain the Bridgeport Series II CNC Milling, Drilling and Boring machine with Bridgeport Operating System Software (BOSS) Level 6.0. Our intention is to provide the resources for diagnosing mechanical or computer problems as well as to provide the means to solve them.

We also address the prevention of problems with a checklist of preventive maintenance procedures. Be sure to read and follow all preventive maintenance procedures shown in Section 9.

This manual is geared to meet the needs of three levels of maintenance, defined as follows:

Level 1 (Operator) The machine operator (or other customer representative) is not assumed to have any detailed knowledge of the equipment. The operator is not assumed to use electrical tools for maintenance.

Level 1 maintenance consists of keeping the equipment clean, lubricating and ensuring that lubricant reservoirs are full, making sure that power is turned on, and following proper startup and operating procedures.

Level 1 personnel are not authorized to make adjustments or replace components.

Level 2 (Dealer Service or specially trained customer personnel) Level 2 service personnel are assumed to have a fair knowledge of the equipment. They are assumed to have VOMs, spare fuses, printed circuit boards and diagnostic tapes.

Level 2 maintenance consists, in addition to all Level 1 procedures, of adjustment of power supply voltages and replacement of major subassemblies, such as step motors, cables, PC boards, fuses, etc., plus certain individual components such as contactors, power switches and disconnects.

Level 2 personnel are not authorized to adjust clock rates or to replace individual components other than those enumerated above.

Level 3 (BMI Field Service or other specially trained personnel) Level 3 maintenance personnel are trained at Bridgeport service school. They are expected to have a detailed knowledge of the equipment and theory of operation.

Level 3 maintenance personnel are equipped with all the tools available to Level 2 personnel plus oscilloscopes and logic probes.

Level 3 maintenance personnel are authorized to perform, in addition to all Level 2 maintenance functions, adjustment of clock rates and replacement of certain individual components such as power semiconductors, filter capacitors, and integrated circuits.

1.2 SCOPE

Sections 1 through 14 of this manual consist of two main parts: Control and Machine.

Sections concerning the Control, provide a theory of operation of the control system, the power distribution, description of the PC boards, the axis drive system, troubleshooting procedures and tests. Maintenance procedures are Level 2 and 3.

The Machine sections concerning the theory of operation, contain preventive maintenance and information on mechanical maintenance and parts replacement. Most of these procedures are Level 1 and 2.

The Appendix contains parts lists. The Machine lists are organized by assembly; the Control lists are organized by function, e.g. electro-mechanical parts, resistors, cables, etc. The Appendix also contains the wiring diagrams, block diagrams and schematics specially segmented for clarity.

1.3 REFERENCED MANUALS

The following manuals for this machine are referenced:

M-142 Installation Manual
M-140 Operating Manual
M-139 Programming Manual

1.4 SPECIFICATIONS

RANGE	INCH	METRIC
Table Travel (X Axis)	30″	(760mm)
Saddle Travel (Y Axis)	15 ″	(380mm)
Quill Travel (Z Axis)	5″	(127mm)
Knee Travel (Manual)	13-3/16″	(337mm)
Throat Distance	15-9/16″	(395mm)
Table to Spindle Gage Line Minimum	7″	(177mm)
Maximum Vertical Load Uniform Distribution	1000 Lbs.	(454kg)

TABLE		
Overall Size	47x16-5/8″	(1195x425mm)
Working Surface	38x15″	(960x380mm)
T-Slots	3 on 4-3/8″ Centers	(3 on 111.125mm centers)
T-Slot Size	5/8″	(15mm)
Position Speed	100 ipm	(2540mm/min)
Height Above Floor-Maximum	50″	(1270mm)

SPINDLE

Motor Rating	2 HP	(1.5kw)
Power Rating	1-1.75 HP	(.75-1.4kw)
Taper	#30 Quick Change	or #200 Universal (optional)
Speed Range	60-4200 RPM	
Transmission Ratios	1:1 and 8.3:1	
Rapid Approach Rate (Z Axis)	100 ipm	(3048mm/min)
Controlled Downfeed Range (Z Axis)	.2-51.0 ipm	(5-1295mm/min)
Drilling Capacity-Mild Steel	3/4" Diameter	(19mm dia.)
Milling Capacity-Mild Steel	1.5 cu. Ins/min	(25cc/min)
Boring Range	To 4" Diameter	(To 102mm dia.)
Tapping Range W/tapping attachment	#5-40 TO 1/2-13	
Spindle Diameter	1-3/8"	(35mm)
Quill Diameter	3-3/8"	(86mm)

MILLING

Feedrate	.2-51.0 ipm	(2-1295mm/min)
Feed Increments	.1 ipm	(1mm/min)
Override-Infinitely Variable	1-120% Constant To 51 ipm	(1295mm/min)
Vector Feedrate Control (XYZ)		

POSITIONING

Rapid Traverse XYZ	100 ipm	(2540mm/min)

MACHINE AND CONTROL PERFORMANCE

Positioning Accuracy	+/– .001" in center 24"	
Positioning Repeatability	+/– .0005"	(0.013mm)
Output Resolution	.0005"	(0.013mm)
Input Resolution	.0001"	(0.001mm)
Jog Increments	1",.1", .01", .0005"	(After serial #9100, 10mm, 1mm, .1mm, .0005mm)

CONTROL SYSTEM

Control Power Supply-60 Hz, 3 Phase	208V/230V/460V (see total power below)
Control Power	12a/6a per phase
Power Requirements (3-Axis)	2.7 KVA
System	Abs/Incremental CNC, Rectangular or Polar Coordinate Input
Format	Word Address Variable Block
Format Detail	n5g2X + 34Y + 34Z + 34R34A + 33i34j34k34f21S4t2m2
Reference EIA Standards	RS-227,RS-274C,RS-358

CNC FEATURES

Storage Capacity	80 ft of equivalent EIA RS-358 tape
Subroutines	36 Macros
Repetitive Programming	4 Levels of nested loops
Transformation	Rotation or Scaling
Editing	20 Command characters
Part Program Loading	Tape Reader (optional) or Data Input Device
Data Input Device	Serial Line Interface @ 20 ma or RS-232
Maintenance	Diagnostic Routines

SPACE AND WEIGHT

Floor Area	80" X 70"	(2032X1778mm)
Height	89"	(2260mm)
Weight (W/control)	5000 lbs.	(2272kg)
Shipping Weight	5400 lbs.	(2455kg)

POWER

Electrical Supply-60 Hz, 3 Phase	230V/460V Single Connection or 208V on Special Order
Main Power Breaker	20A/10A per phase
Electrical Rating	5KVA

COLOR

Standard	Machine Tool Gray

2.3 LSI-11 PROCESSOR

2.3.1 Operation

Figure 2-2 shows a simplified computer structure. In general, the processor consists of various functional parts:

1. A programmable arithmetic/logic unit (ALU) that can act as many of the logic elements used in a random logic system. For example, it can add, subtract, increment, decrement, AND, OR, and compare the result of an operation to zero.
2. Processor control logic that analyzes the various programmed instructions and causes the system to generate a sequence of events which will execute the instruction.
3. Bus Input/Output control that enables communication to and from the processor.

Two types of information are passed through the bus: the address and the data. The address is the physical location of the data to be used.

2.3.2 Addressing Memory

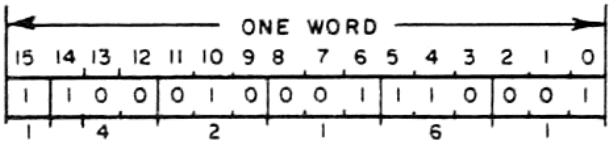
Figure 2-3 shows a memory map of the Series II CNC system. Note that the LSI-11 uses a 16 bit word. This means that 65,536 unique locations can be directly addressed. However, the LSI-11 directly addresses both bytes (8 bits) and words (16 bits). An LSI-11 word consists of a high byte and a low byte.

Word addresses are always even numbered. Byte addresses can be either even or odd numbered. Low bytes are stored at even numbered memory locations and high bytes at odd-numbered memory locations.

Considering the system as word organized, the LSI-11 can directly address 32K words.

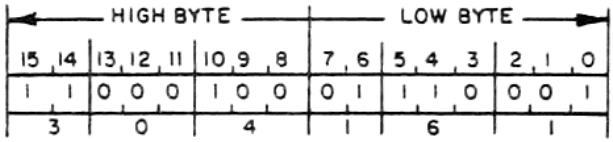
NOTE

For convenience, values will be given in octal code. A 16-bit word would be represented as follows:



This is 142161 in octal.

The same data as 2 bytes would be:



161 - low byte
304 - high byte

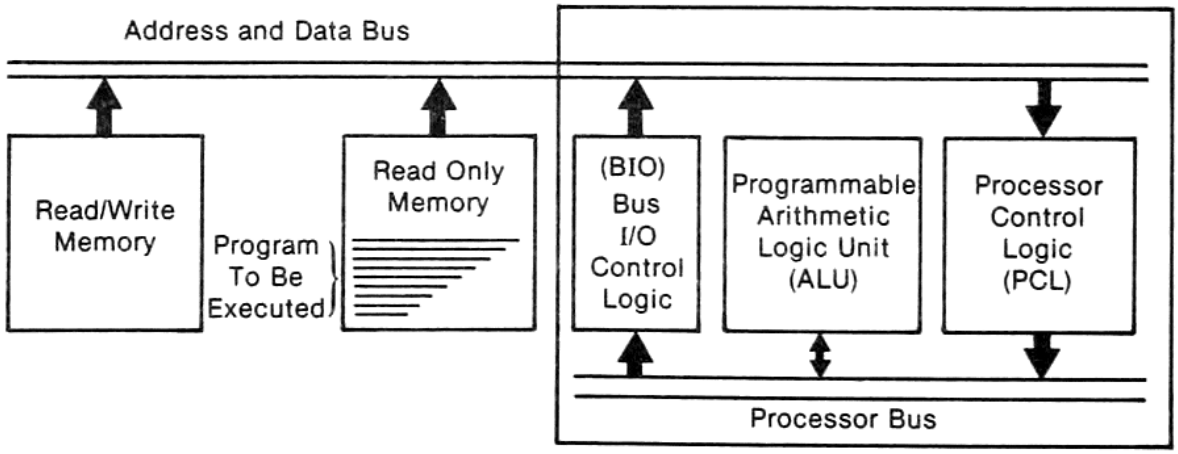


Figure 2-2 Simplified Computer Structure

Data can be of two kinds:

1. Data to be operated on by the system. For example, the value 2.
2. Instructions to be executed by the system. For example, the instruction ADD, A, B, would be 066767.

2.3.3 Program Levels

There are three hierarchical levels of program instructions in the Series II CNC system:

1. The micro program. It tells the processor how to execute a particular instruction. The micro program can only be modified by DEC.
2. The macro program. BOSS (Bridgeport Operating Software System) is a set of instructions that make the system perform as an NC. BOSS is contained in read only memory, and should only be modified by Bridgeport-Textron.
3. The part program. This is input by the user to cause the control to machine a work piece.

2.4 LSI-BUS

2.4.1 Lines

The LSI-11 Bus consists of 17 control lines and a 16 line data/address bus. Address/data and control lines are open collector lines which are asserted low.

2.4.2 Pin Assignments—Figure 2-4

Table 2-1 shows the bus pin assignments. Each slot shown as ROW A and ROW B in Figure 2-4, includes a numeric identifier for the side of the module. The component side is designated side "1" and the solder side is designated side "2". Letters ranging from A through V (excluding G, I, O, Q) identify a particular pin on a side of a slot.

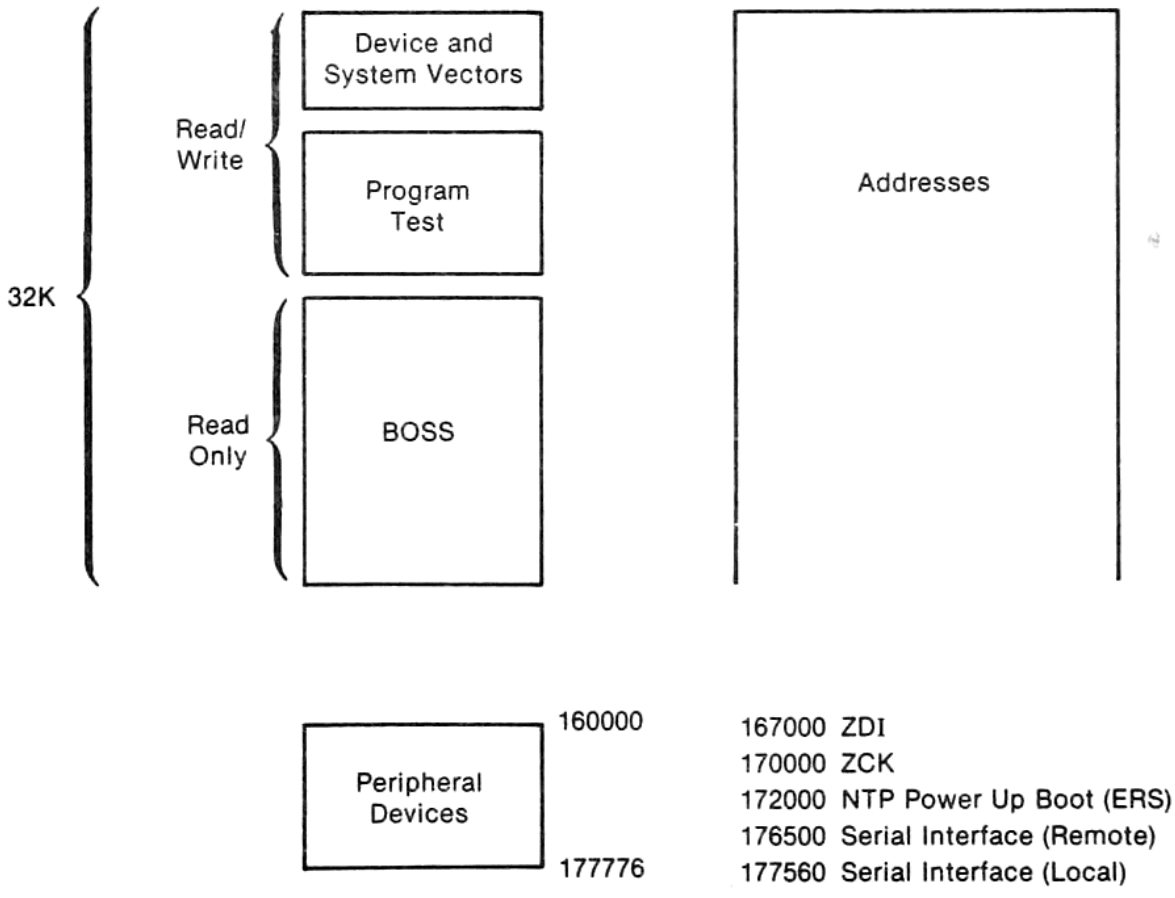


Figure 2-3 Map of BOSS 6

A typical pin is designated as:

B E 2
SLOT (ROW) INDENTIFIER
"SLOT B"

PIN IDENTIFIER
"PIN E"

MODULE SIDE IDENTIFIER
"SOLDER SIDE"

All slot A pins are connected on the backplane to the corresponding slot C pins. All slot B pins are connected on the backplane to the corresponding slot D pins. Refer to Drawing 1040213.

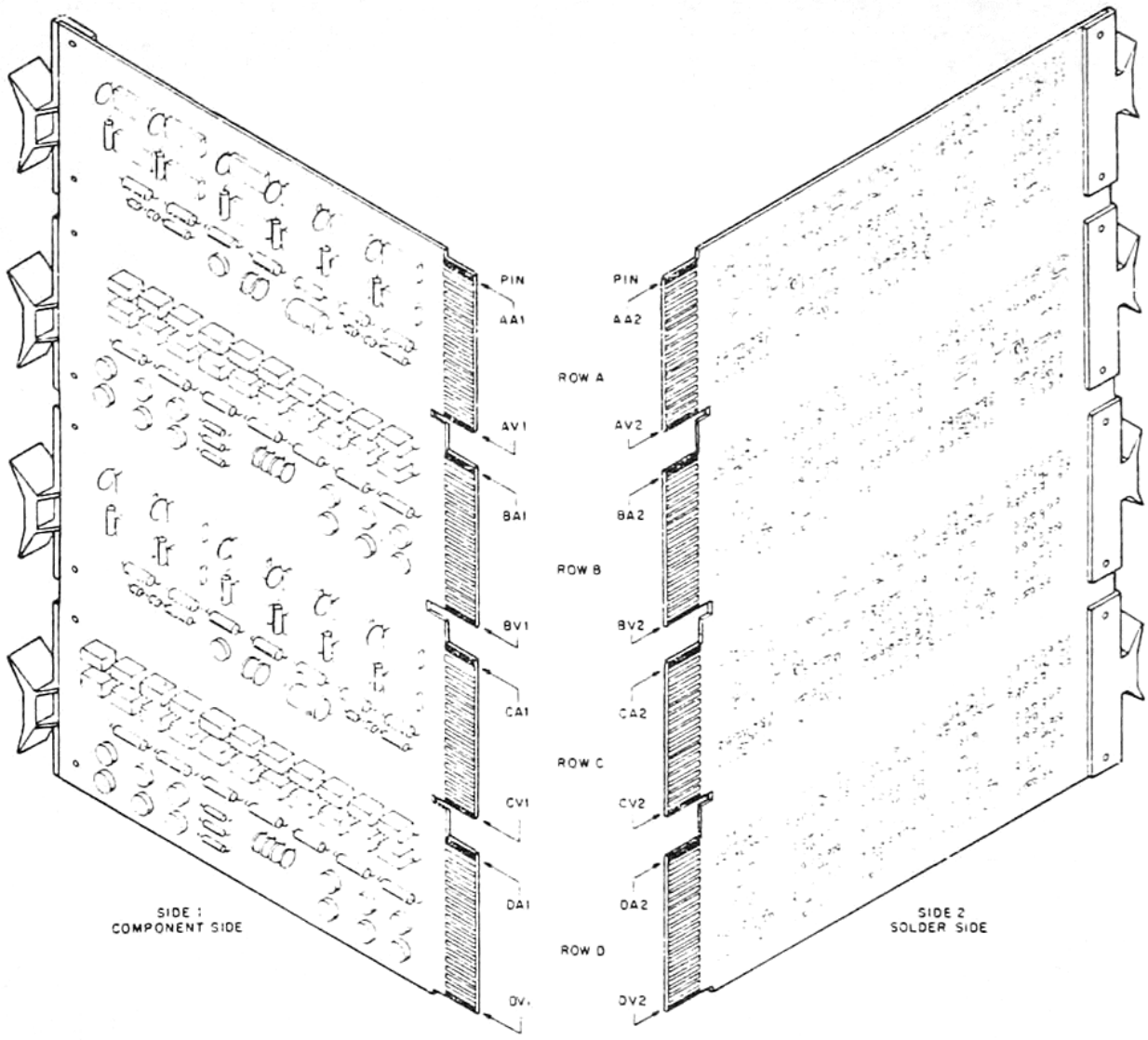


Figure 2-4 LSI-11 Pin Assignments

TABLE 2-1 LSI-11 PIN ASSIGNMENTS

BUS PIN	MNEMONIC	DESCRIPTION
AA1	BSPARE1	
AB1	BSPARE2	
AC1	BSPARE3	**Bus Spares** (Not assigned. Reserved for DIGITAL use).
AD1	BSPARE4	
AE1	SSPARE1	**Special Spares**
AF1	SSPARE2	(Not connected to LSI-11.
AH1	SSPARE3	Connected to other sockets.)
AJ1	GND	**Ground:** System signal ground and DC return.
AK1	MSPAREA	**Maintenance Spares**
AL1	MSPAREA	(Not connected to LSI-11. Connected to other sockets.)
AM1	GND	**Ground:** System signal ground and DC return.
AN1	BDMR L	**Direct Memory Access (DMA) Request:** A device asserts this signal to request bus mastership. The processor arbitrates bus mastership between itself and all DMA devices on the bus. If the processor is not bus master (it has completed a bus cycle and BSYNC L is not being asserted by the processor), it grants bus mastership to the requesting device by asserting BDMGO L. The device responds by negating BDMR L and asserting BSACK L.
AP1	BHALT L	**Process or Halt:** When BHALT L is asserted, the processor responds by halting normal program execution. External interrupts are ignored but memory refresh interrupts (enabled if W4 on the process module is removed) and DMA request/grant sequences are enabled. When in the halt state, the processor executes the ODT microcode and the console device operation is invoked.
AR1	BREF L	**Memory Refresh:** Asserted by processor microcode-generated refresh interrupt sequence (when enabled) or by an external device. This signal forces all dynamic MOS memory units to be activated for each BSYNC L/BDIN L bus transaction.
AS1	PSPARE3	**Spare** (Not assigned. Customer usage not recommended).
AT1	GND	**Ground:** System signal ground and DC return.
AU1	PSPARE1	**Spare** (Not assigned. Customer usage not recommended).
AV1	+5B	**+5V Battery Power:** Secondary +5V power connection. Battery power can be used with certain devices.
BA1	BDCOK H	**DC Power OK:** Power supply-generated signal that is asserted when there is sufficient DC voltage available to sustain reliable system operation.
BB1	BPOK H	**Power OK:** Asserted by the power supply when primary power is normal. When negated during processor operation, a power fail trap sequence is initiated.
BC1	SSPARE4	
BD1	SSPARE5	
BE1	SSPARE6	Not connected to LSI-11.
BF1	SSPARE7	Connected to other sockets.
BH1	SSPARE8	
BJ1	GND	**Ground:** System signal ground and DC return.
BK1	MSPAREB	Not connected to LSI-11.
BL1	MSPAREB	Connected to other sockets.
BM1	GND	**Ground:** System signal ground and DC return.
BN1	BSACK L	This signal is asserted by a DMA device in response to the processor's BDMGO L signal, indicating that the DMA device is bus master.
BP1	BSPARE6	**Bus Spare** (Not assigned, Reserved for DIGITAL use).
BR1	BEVNT L	**External Event Interrupt Request:** When asserted, the processor responds (if PS bit 7 is 0) by entering a service routine via vector address 100. Used in I-CNC for feedrate clock pulse interrupt.
BS1	PSPARE4	**Spare** (Not assigned. Customer usage not recommended).
BT1	GND	**Ground:** System signal ground and DC return.
BU1	PSPARE2	**Spare** (Not assigned. Customer usage not recommended).

BV1	+5	**+5V Power:** +5V DC system power.
AA2	+5	**+5V Power:** Normal +5V DC system power.
AB2	−12	**−12V Power:** −12 DC optional power for devices requiring this voltage.
AC2	GND	**Ground:** System signal ground and DC return.
AD2	+12	**+12V Power:** +12V DC system power.
AE2	BDOUT L	**Data Output:** BDOUT, when asserted, implies that valid data is available on BDALO-15 L and that an output transfer, with respect to the bus master device, is taking place. BDOUT L is deskewed with respect to data on the bus. The slave device responding to the BDOUT L signal must assert BRPLY L to complete the transfer.
AF2	BRPLY L	**Reply:** BRPLY is asserted in response to BDIN L or BDOUT L and during IAK transactions. It is generated by a slave device to indicate that it has input data available on the BDA L bus or that it has accepted output data from the bus.
AH2	BDIN L	**Data Input:** BDIN is used for two types of bus operations: 1. When asserted during BSYNC L time, BDIN L implies an input transfer with respect to the current bus master, and requires a response BPPLY L. BDIN L is asserted when the master device is ready to accept data from a slave device. 2. When asserted without BDYNC L, it indicates that an interrupt operation is occurring. The master device must deskew input data from BRPLY L.
AJ2	BSYNC L	**Synchronize:** BSYNC L is asserted by the bus master device to indicate that it has placed an address on BDALO-15 L. The transfer is in process until BSYNC L is negated.
AK2	BWTBT L	**Write/Byte:** BWTBT L is used in two ways to control a bus cycle: 1. It is asserted during the leading edge of BSYNC L to indicate that an output sequence is to follow (DATO or DATOB), rather than an input sequence. 2. It is asserted during BDOUT L, in a DATOB bus cycle, for byte addressing.
AL2	BIRQ L	**Interrupt Request:** A device asserts this signal when its Interrupt Enable and Interrupt Request flip-flops are set. This signal informs the processor that a device has data to input to the processor or it is ready to accept output data. If the processor's PS word bit 7 is 0, the processor responds by acknowledging the request by asserting BDIN L and BIAKO L.
AM2	BIAKI L	**Interrupt Acknowledge Input and Interrupt Acknowledge Output:** This is an interrupt acknowledge signal which is generated by the processor in response to an interrupt request (BIRQ L). The processor asserts BIAKO L, which is routed to the BIAKI L pin of the first device on the bus. If it is requesting an interrupt, it will inhibit passing BIAKO L. If it is not asserting BIRQ L, the device will pass BIAKI L to the next (lower priority) device via its BIAKO L pin and the lower priority device's BIAKI L pin.
AP2	BBS7 L	**Bank 7 Select:** The bus master asserts BBS7 L when an address in the upper 4K bank (address in the 28-32K range) is placed on the bus. BSYNC L is then asserted and BBS7 L remains active for the duration of the addressing portion of the bus cycle.
AR2 AS2	BDMGI L BDMGO L	**DMA Grant Input and DMA Grant Output:** This is the processor generated daisy chained signal which grants bus mastership to the highest priority DMA device along the bus. The processor generates BDMGO L, which is routed to the BDMGI L pin of the first device on the bus. If it is requesting the bus, it will inhibit passing BDMGO L. If it is not requesting the bus, it will pass the BDMGI L signal to the next lower priority device via its BDMGO L pin. The device asserting BDMR L is the device requesting the bus, and it responds to the BDMGI L signal by negating BDMR, asserting BSACK L, assuming bus mastership, and executing the required bus cycle.
AT2	BINIT L	**Initialize:** BINIT is asserted by the processor to initialize or clear all devices connected to the 1/0 bus. The signal is generated in response to a power-up condition (the negated condition of BDCOK H).

AU2	BDALO L	**Data/Address Lines:** These two lines are part of the 16-line data/address bus over which address and data information are communicated. Address information is first placed on the bus by the master device. The same device then either receives input data from, or outputs data to the addressed slave device or memory over the same bus lines.
AV2	BDAL1 L	
BA2	+5	**+5V Power:** Normal +5V DC (optional) power for devices requiring this voltage.
BC2	GND	**Ground:** System signal ground and DC return.
BD2	+12	**+12V Power:** +12V system power
BE2	BDAL2 L	
BF2	BDAL3 L	
BH2	BDAL4 L	
BJ2	BDAL5 L	
BKS	BDAL6 L	
BL2	BDAL7 L	Data/Address Lines:
BM2	BDAL8 L	These 14 lines
BN2	BDAL9 L	are part of the 16-line data/address
BP2	BDAL10 L	bus previously described.
BR2	BDAL11 L	
BS2	BDAL12 L	
BT2	BDAL13 L	
BU2	BDAL14 L	
BV2	BDAL15 L	

2.4.3 Bus Cycles—Figures 2-5, 2-6, 2-7

Overview Every processor instruction requires one or more I/O (input/output) operations. The first operation required is a data input transfer (DATI), which fetches an instruction from the location addressed by the program counter (PC or R7). This operation is called a DATI bus cycle. If additional operations are not referenced in memory or in an I/O device, no additional bus cycles are required for instruction execution. However, if memory or a device is referenced, additional DATI, data input/output (DATIO or DATIOB), or data output transfer (DATO or DATOB) bus cycles are required. Between these bus cycles, the processor can service DMA requests. However, the processor can service interrupt requests only prior to an instruction fetch (DATI bus cycle), and only if the processor's priority is zero (PS word bit 7 is 0).

The following paragraphs describe the types of bus cycles. Note that the sequences for I/O operations between processor and memory or between processor and I/O device are identical. DATO (or DATOB) cycles are equivalent to write operations, and DATI cycles are equivalent to read operations. In addition, DATIO cycles include an input transfer followed by an output transfer. The DATIO cycle provides an efficient means of executing an equivalent read-modify-write operation by making it unnecessary to assert an address a second time.

Input Operations—Figures 2-6, 2-7—The sequence for a DATI operation is shown in Figure 2-5. DATI cycles are asynchronous and require a response from the addressed device or memory. The addressed memory or device responds to its input request (BDIN L) by asserting BRPLY L. If BRPLY is not asserted within 10 uS (max) after BDIN L is asserted, the processor terminates the cycle and traps through location 4.

Note that BWTBT L is not asserted during the address time, indicating that an input data transfer is to be executed.

A DATIO cycle is equivalent to a read-modify-write operation. An addressing operation and an input word transfer are first executed in a manner similar to the DATI cycle; however, BSYNC L remains in the active state after completing the input data transfer. This causes the addressed device or memory to remain selected, and an output data transfer follows without any further addressing. After completing the output transfer, the device terminates BSYNC L, completing the DATIO cycle. The actual sequence required for a DATIO cycle is shown in Figure 2-6. Note that the output data transfer portion of the bus cycle can be a byte transfer; hence, this cycle is shown as DATIOB.

Output Operations—Figures 2-6, 2-7—The sequence required for a DATO or the equivalent output byte (DATOB) bus cycle is shown in Figure 2-7. Like the input operations, failure to receive BRPLY L within 10 uS after asserting BDOUT L is an error, and results in a processor time-out trap through location 4.

Note that BWTBT L is asserted during the addressing portion of the cycle to indicate that an output data transfer is to follow. If a DATOB is to be executed, BWTBT L remains active for the duration of the bus cycle; however, if a DATO (word transfer) is to be executed, BWTBT L is negated during the remainder of the cycle.

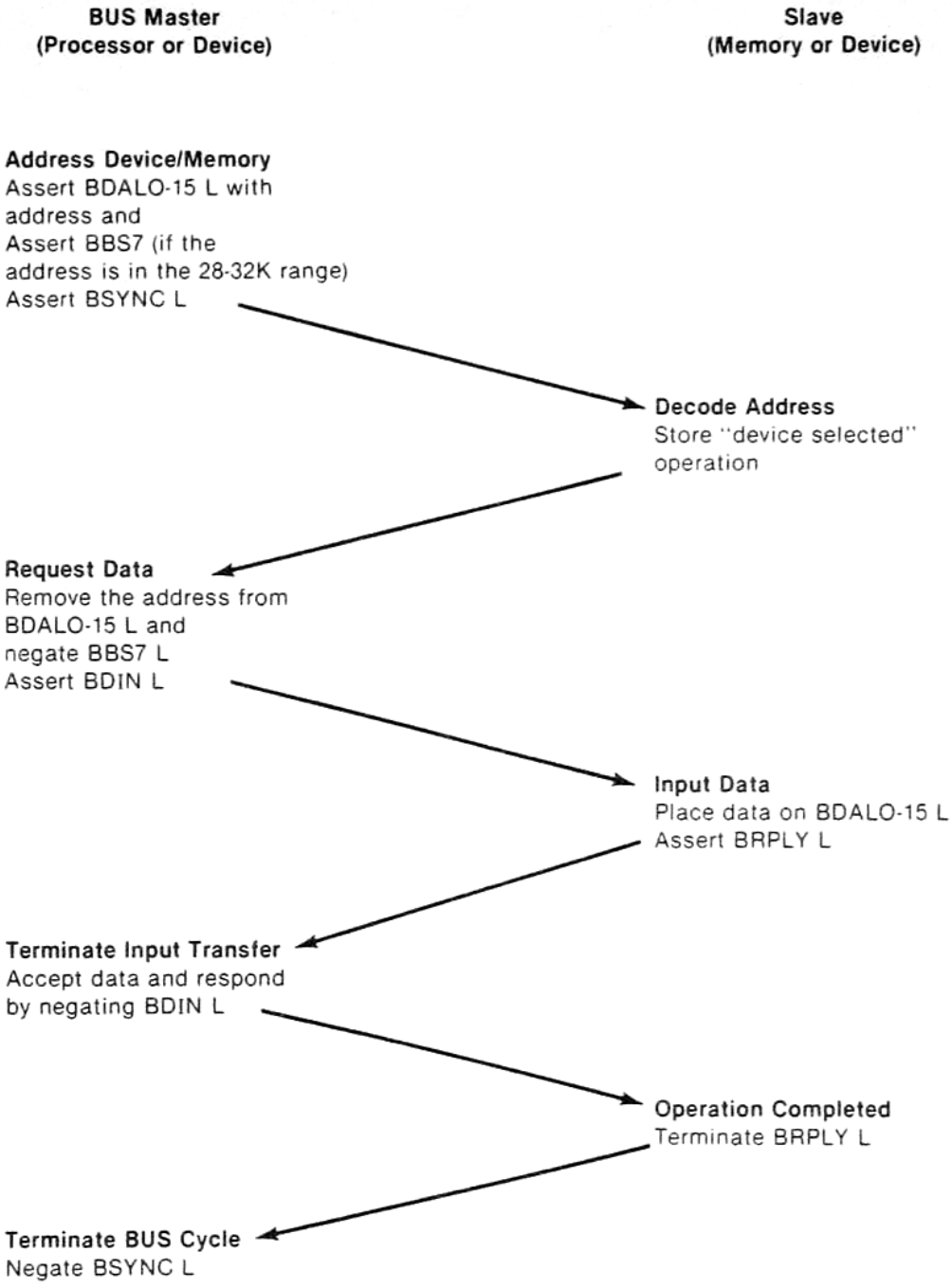


Figure 2-5 DATI Bus Cycle

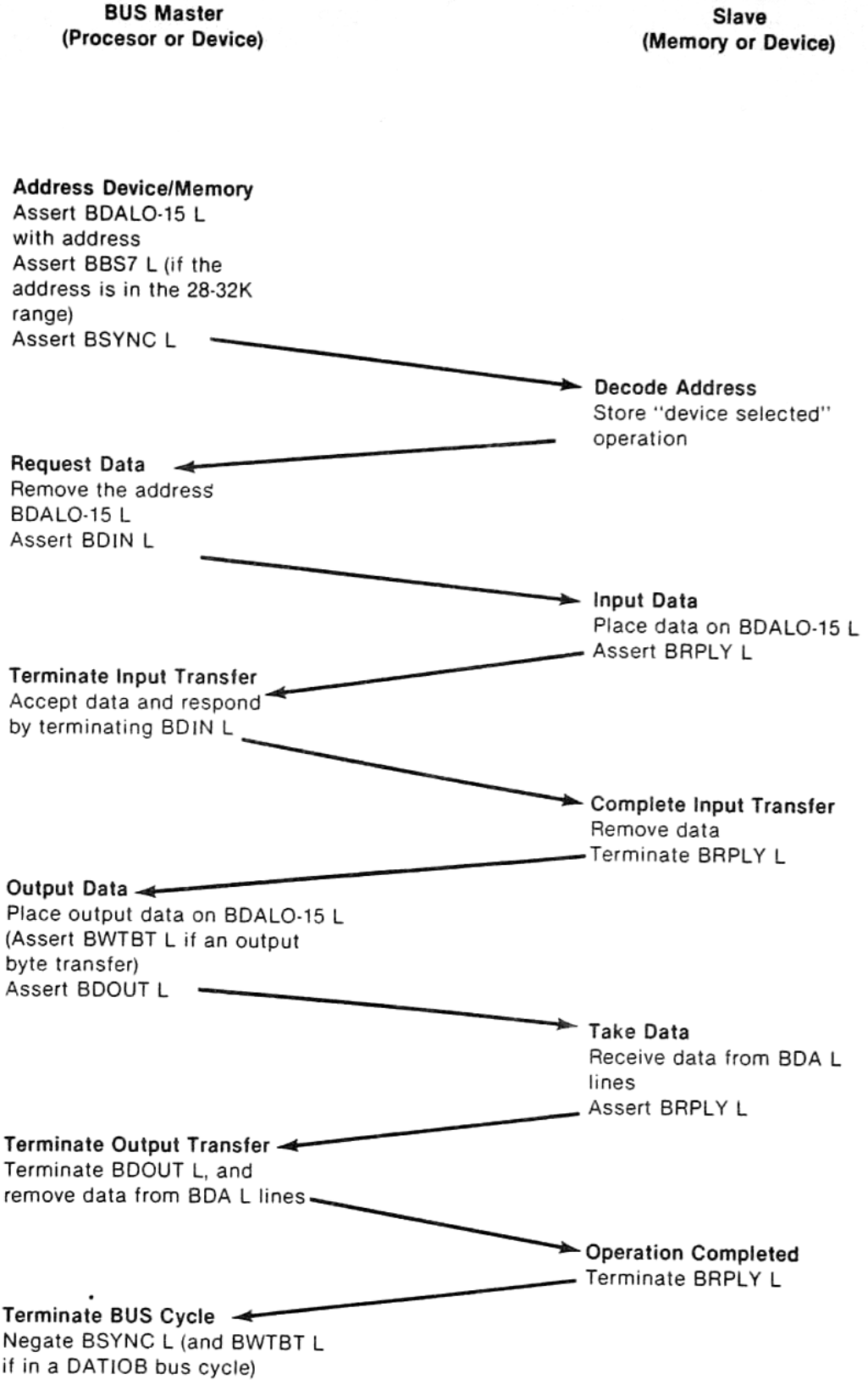


Figure 2-6 DATIO or DATIOB Bus Cycle

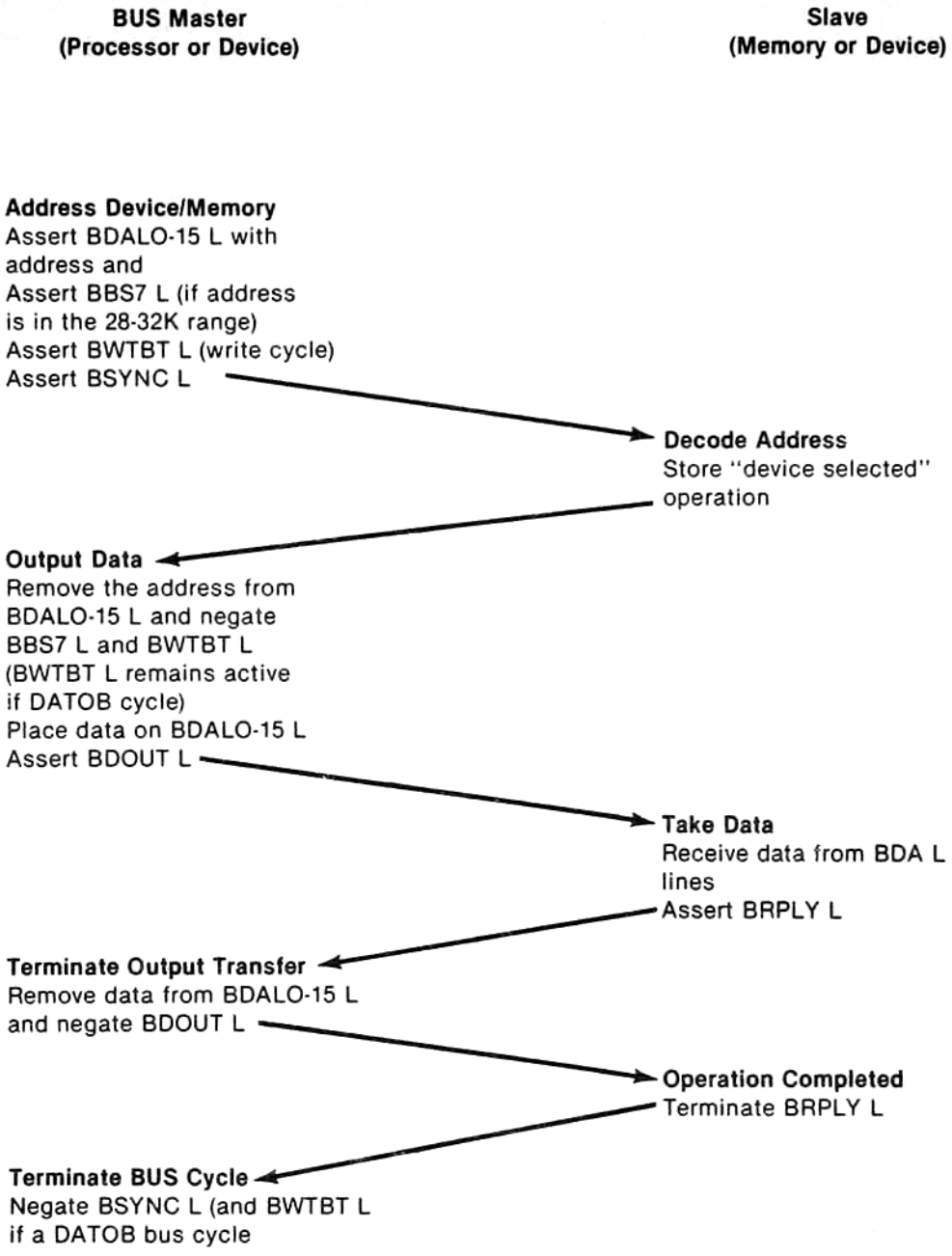


Figure 2-7 DATO or DATOB Bus Cycle

2.4.4 Interrupts—Figure 2-8

Overview Interrupts are requests made by peripheral devices which cause the processor to suspend temporarily its present program execution and jump to the service routine for the particular interrupt. After completing the service routine, program control is restored to the interrupted program.

An interrupt vector associated with each device is hard wired into the device's interface control logic. This vector is an address pointer that allows automatic entry into the service routine. For example, the front panel keyboard generates an interrupt each time a key is depressed. The vector for the front panel keyboard is 70.

When the processor recognizes the interrupt it stores the condition of the system so that after the interrupt is completed, the program will resume exactly where it left off.

This involves pushing the processor status word (PSW) and the program counter (PC) onto the system stack.

The effect is:

push PSW on stack
push PC on stack

The new contents of the PC and PSW are loaded from two preassigned consecutive memory locations which are called an "interrupt vector". The first word contains the interrupt service routine address (the jump to location), the second word contains the new PSW which will determine the machine status including the operational mode to be used by the interrupt service routine.

After the interrupt service has been completed, a R11 return from interrupt is performed. The two top words on the "stack" are automatically "popped" and placed in the PC and PSW respectively, thus resuming the interrupted program.

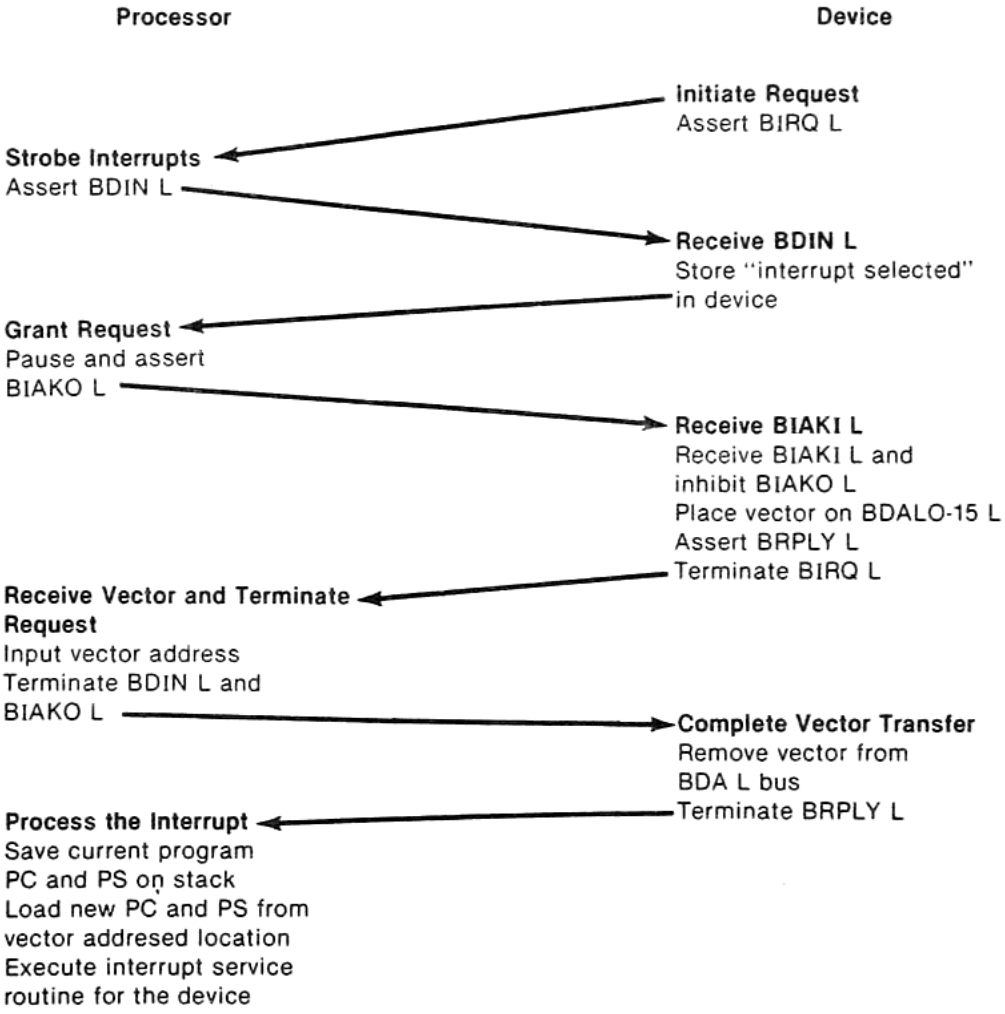


Figure 2-8 Interrupt Request/Acknowledge Sequence

Routines—Figure 2-8

BOSS 6 uses 8 interrupt routines:

1. 10T (Vector 20)
   Used for I/O subroutines
2. Traps (Vector 34)
   Used to invoke system subroutines
3. ZAXIT (Vector 54)
   Used for Z axis subroutines
4. YAXIT (Vector 60)
   Used for Y axis subroutines
5. XAXIT (Vector 64)
   Used for X axis subroutines
6. External Switch (Vector 70)
   This is actuated by the front panel pushbutton switches, the MDI keyboard, the EMERGENCY STOP pushbutton, and the CLEAR switch paper tape load. Also vector 70 is armed in AUTO and GO TO when the spindle contactor is disconnected.
7. Transfer Buffer to Active (Vector 74)
   This is armed by Buffer Full and the active arithmetic logic = 0.
8. End of Move (Vector 100).

The interface control and data signal sequence required for interrupts is shown in Figure 2-8. A device requests interrupt service by asserting BIRQ L. The processor can acknowledge interrupt requests only between instruction executions by generating an active (low) BDIN L signal, enabling the device's vector response. The processor then asserts the BIAKO L signal.

The first device on the bus receives this daisy-chained signal at its BIAKI L input. If it is not requesting service, it passes the signal via its BIAKO L output to the next device, and so on, until the requesting device receives the signal. The device that did not pass the BIAKO L signal responds by asserting BRPLY L (low) and placing its interrupt vector on data/address bus lines BDALO-15 L. Automatically entry to the service routine is then executed by the processor as previously described. If a device fails to assert BRPLY L in response to BDIN L within 10 uSec, the processor enters the Halt state.

Automatic entry to the service routine is then executed by the processor as described above.

SECTION 3
POWER DISTRIBUTION

3.1 POWER

Prime power to the system is 3-phase 50 Hz or 60 Hz AC. Input Voltage is selected by the customer when ordering the machine. Input voltage can be changed in the field by use of a voltage conversion kit. Available voltages are:

Voltage (Volts)	Frequency (Hertz)
208	60
230	50
230	60
380	50
416	50
420	50
460	50
460	60
575	60

Three-phase power enters the system through the main system disconnect located on the Power Equipment Enclosure, and feeds the three-phase distribution wiring.

Items connected to the three-phase distribution are:

1. Reversing contactor and spindle motor
2. 125V single phase 1KVA transformer (T1)
3. Axis drive power transformer (T2)

3.1.1 Single Phase Power

The 125V single phase output from T1 feeds the single phase distribution wiring. Items fed from this distribution are as follows:

1. Reversing contactor
2. Lube pump motor
3. Tape reader (when included)
4. Fans
5. 24VDC supply (T7)
6. 56VDC supply (T6)
7. Regulated power supply (T8)
8. Flood coolant triac (when included)

3.1.2 24VDC Power

The 24VDC power is used for general purpose switching and control functions in which close voltage regulation is not important. These include:

1. The SMD boards
2. The ACC board
3. Control relays CR1, CR2 and CR3 (when included)
4. The SCA board (in part)
5. Incandescent indicators

3.2. REGULATED POWER SUPPLY ADJUSTMENT

The regulated power supply has three output voltages; +5V, +12V and −12V. Procedures for adjustment are given in Section 6.3, Troubleshooting.

Note

Refer to the System Wiring Diagrams 1040338, Sheets 1-5 at the end of this section.

SECTION 4
LOGIC BOARDS

4.1 INTRODUCTION

This section provides a detailed explanation of the logic circuits, switches and addresses as well as the interrelating functions of the following boards: UFP, ZDI, NTP, ZCK, ERS AND SCA.

The explanations are given to help you locate trouble areas. Most procedures indicated or implied in this section, such as probing for signals, are maintenance level 3 procedures. Do not attempt to repair the boards. Once you have discovered that a board is defective, replace it and send it back to Bridgeport Controls.

The material in this section makes reference to schematics located at the end of this section. We have segmented them for referral as the text explains the various elements that comprise each board.

4.2 UNIVERSAL FRONT PANEL (UFP) LOGIC BOARD

4.2.1 Interfacing Function

The UFP board is the interface between the Operator's Main Control Panel (Figures 4-1, 4-2) and the ZDI Board. It performs two functions: data input and data output.

1. **Data Input** It multiplexes and selects data from all the Operator's Main Control Panel switches (except the OVERRIDE controls) and transfers the selected data to the ZDI board.
2. **Data Output** Its receives status, data and control signals from the ZDI board to drive the necessary displays in the Operator's Main Control Panel.

Figure 4-1 Operator's Main Control Panel S/N 7000 to S/N 7409

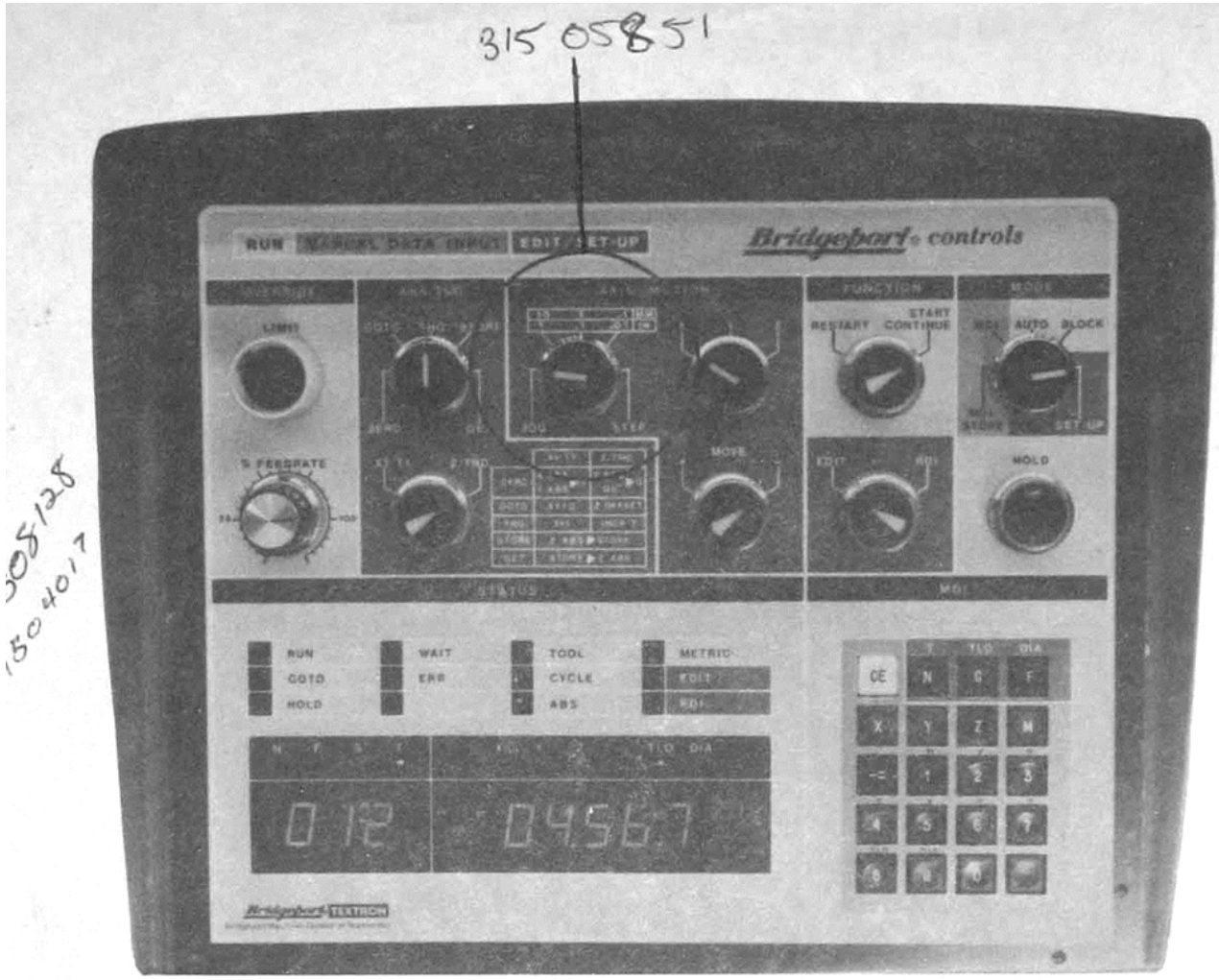


Figure 4-2 Operator's Main Control Panel S/N 7410 and After

Data Input Section (Switch Interface)—Figure 4-3

There are two groups of switches: sustained position and momentary action switches.

1. Sustained Position switches entering and UFP board through K2:
   a. S1, the MODE switch (5-position selector)
   b. S3, the AXIS MOTION (X, Y or Z) switch (3 position selector)
   c. S4, the JOG STEP switch (5 position selector JOG 1″, .1″, .01″, .0005″); after serial #9100, JOG STEP is metric (JOG 10mm, 1mm, .1mm, .0005mm)
   d. S5, the ABS/TLO switch (5 position selector)
   e. S9, (right side), the MOVE switch (2 position selector pushbutton)
   f. S6, the LIMIT OVERRIDE switch. It contains a lamp and a momentary action pushbutton. These do not connect to the UFP board but go directly to the Axis Limit circuits in the Control Equipment Enclosure.
2. Momentary Action Switches (entering through K4 and K5):
   a. S2, the FUNCTION switch (2 position selector pushbutton)
   b. S7, the HOLD switch (momentary action pushbutton)
   c. S8, the EDIT/RDI switch (2 position selector pushbutton)
   d. S9, (left side), the pushbutton portion of the AXIS MOTION switch. The output of this switch passes through the UFP board to the XDI with little processing.
   e. S10, the XY/T1-Z/TNO switch (2 position selector pushbutton)
   f. The MDI keyboard, twenty momentary action keys in a 4 × 5 matrix.

The multiplex circuits route the outputs of these switches to the ZDI board, the desired data being selected

by the multiplex address lines FAL1L, FAL2L and FKYSL. Two address ranges are used:

167460 - 167466: these select the first group of switches (FSYSL HIGH)

167470 - 167476: these select the second group of switches (FKYSL LOW)

Data Output (Display Interface)—Figure 4-4

The status and BCD readout data are multiplexed in the ZDI board and fed to UFP K1. The data go to a set of drivers and from there to the status display LEDs. The BCD data are also transmitted over four lines to a BCD to seven segment decoder/driver. From the decoder/driver the data go to the numeric display. The seven segment displays are multiplexed under control of the data multiplex clock in the ZDI at approximately 1KHz. Two address ranges are used:

167604 - 167616: status display (single LEDs)

167620 - 167636: numeric display (seven segment LEDs)

4.2.2 Detailed Circuit Analysis

Switch Multiplex—Drawing 1040223, Sheet 2 shows the circuits for encoding, multiplexing and selecting switch data from the Operator's Main Control Panel. The drawing shows all the operator controls with the exception of the LIMIT OVERRIDE switch. The FEEDRATE OVERRIDE potentiometer is wired through UFP K2 and K3 although the UFP board does not modify it. Another signal that goes through the UFP board without major processing is FJGSWH (JOG) from S9-2L. In the released position S9-2L applies a ground through R28 to ZDI K10-8. When S9 is depressed S9-2L is disconnected from ground and pulled up towards Vcc by R29.

Switches are of four types. Diagrams on the lower left hand corner of Drawing 1040223, sheet 2, show three of these types. The switch number is in parentheses under the applicable switch diagram. The arrows indicate the positions: O means OPEN, X CLOSED, L LEFT, and R RIGHT. Positions are shown as viewed from the front of the Operator's Main Control Panel.

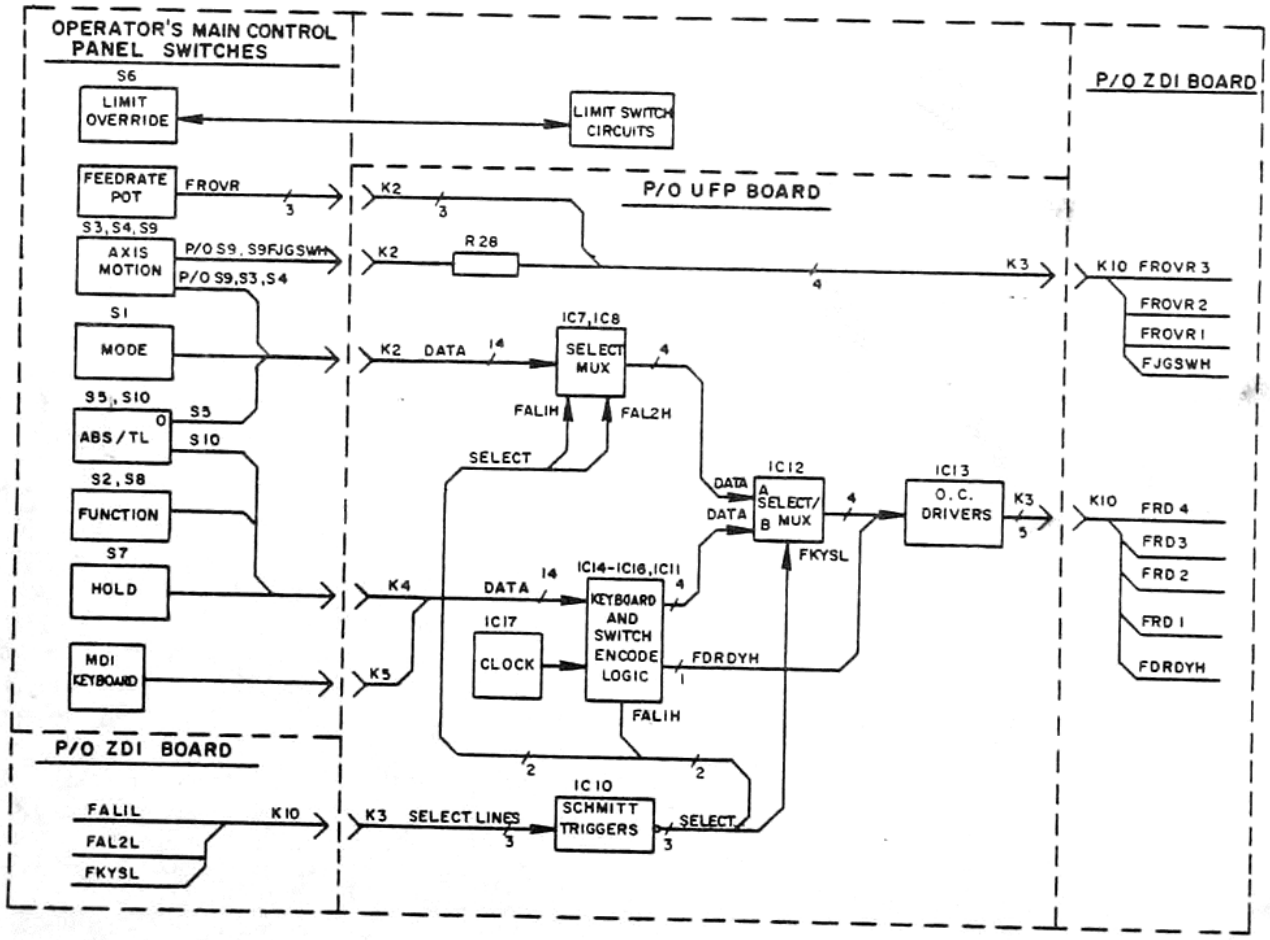


Figure 4-3 UFP Switch Interface

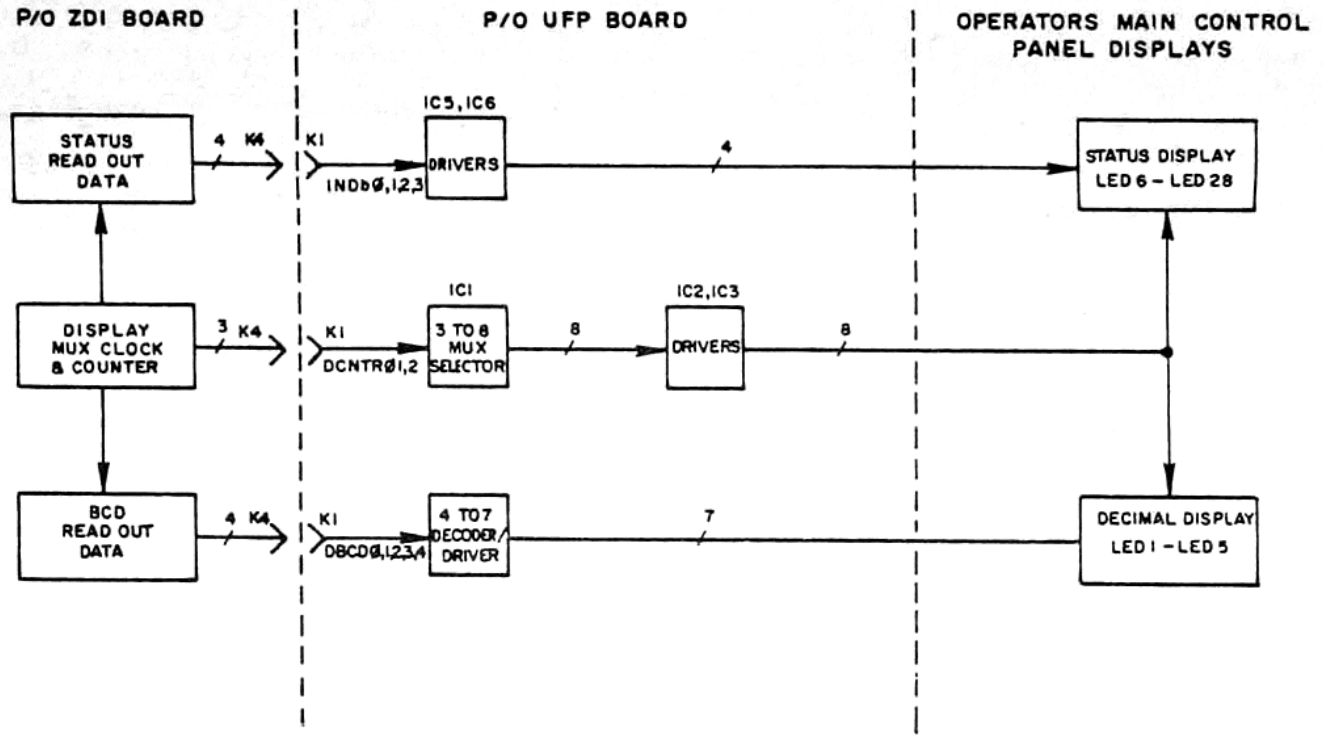


Figure 4-4 UFP Display Interface

S3 uses only the R section. In the CCW position all the contacts are open, in the center position contacts 2 and 1 are closed, and in the CW position contacts 4-3 are closed.

S1, S4 and S5 are five position selectors. The diagram for these switches follows the same convention as that for S3; however, they use both sections.

S2, S8, S9 and S10, are two position selector momentary action pushbutton switches. The selection is made by the R section and the momentary action by the L section; thus in the CCW position contacts 2-1R are closed and in the CW contacts 4-3R are closed. When this switch is released, it closes contacts 2-1L. When pressed, it opens contacts 2-1L and closes 4-3L.

S7 (HOLD) is a momentary action pushbutton switch. When released it opens contacts 3-4 and, when pressed, it closes these contacts.

The MDI keyboard is a 4 by 5 switch matrix with four columns and five rows of pushbutton switches. Drawing 1040223, sheet 2, shows the wiring matrix. The four columns are designated X1 through X4 and the five rows Y1 through Y5. When any switch is pressed a row and a column are simultaneously addressed.

Sustained-Position Switches Excepting the FJGSWH signal from S9-2L, all the switch inputs through UFP K2 are multiplexed by IC7 and IC8. Outputs of the switches feed through K2 and enter the two dual data selector/multiplexers IC7 and IC8. Each of these has two sections, each with four inputs and two outputs. The state of the address inputs A and B determines which pair of input signals are fed to the corresponding outputs.

Note, for example, that the CO inputs (1CO and 2CO) on each IC are connected to the four outputs of S1. Similarly, the C1 inputs connect to S5 and the C2 inputs to S4. The C3 inputs of IC8 connect to S3, while the corresponding inputs of IC7 are not used. Table 4-1 shows the 16 data inputs (each representing a switch position) under the data selection columns, and the four outputs (each representing a switch function) under the switch selection column.

IC9 routes the outputs of IC7 and IC8 to selector IC12. The different signals may be combined in this manner because each switch can only be in one position (and have one output) at a time.

IC12 acts as a switch controlled by address input FKYSL; when FKYSL is high, data from the upper section just described is fed out, while FKYSL is low the lower section is selected.

Momentary Action Switches The operator switches in this group and the MDI keyboard feed to encoder IC14. Note that the MDI keyboard connects only to columns Y1 through Y5. Operator switches S2, S7, S8, S9 and S10 connect to columns Y7 and Y8, and to the same X inputs as the MDI keyboard. In consequence, they are addressed by encoder IC14 as if they were additional MDI keys. Closure bounce is masked by capacitor C9 on IC14-17.

SELECT INPUTS		DATA SELECTION				SWITCH SELECTION (SWITCH FUNCTION)
		IC7		IC8		
B	A	1Y	2Y	1Y	2Y	
L	L	1CØ (BLOCK)	2CØ (SETUP)	1CØ (MDI)	2CØ (AUTO)	S1 (MODE)
L	H	1C1 (STORE)	2C1 (GET)	1C1 (GO TO)	2C1 (TNO)	S5 (ABS/TNO)
H	L	1C2 (.Ø1)	2C2 (STEP)	1C2 (1)	2C1 (1)	(AXIS MOTION)
H	H	1C3 H	2C3 H	1C3 (Y)	2C3 (Z)	S3 (AXIS)

SWITCH POSITIONS AND SWITCH FUNCTION SHOWN IN PARENTHESES

LOGIC LEVELS : L = LOW
H = HIGH

Table 4-1 IC7 and IC8 Data Selection

The control selects priority by scanning the row (X) and column (Y) inputs until the first X-Y closure is found. This avoids ambiguity in case of more than one simultaneous switch closure. The scanning rate is derived from the clock input at IC14-3. The clock frequency is fixed by IC17, R43, R44 and C21 at approximately 21.5kHz. Encoder IC14 has nine data output lines, of which six are used, and a data strobe output (pin 14) which goes low when the encoder receives a switch closure. This strobe signal is fed out to the ZDI board where it is used to generate a computer interrupt.

The six data lines from the encoder are fed to the address inputs of PROMs IC15 and IC16 which translate the encoder output into the CNC internal code. The output of the PROMs goes to selector IC11, where the four lower bits (representing switch type) and the four upper bits (representing switch function) are selected in accordance with address bit FAL1L.

The selected data outputs from IC12 go through open collector driver IC13 to the ZDI board. The strobe signal FDRDYH, generated when any of the switches in Table 4-1 is pressed, also goes through IC13. These five signals are applied to the ZDI Board via a connecting cable from UPF K3 to ZDI K10. The ZDI accepts these data and transfers them to locations 167460 through 167472 (See Table 4-2).

The UFP board receives power from the ZDI board. Vcc, ground and – 12 VDC come from ZDI K10 to UFP K3 as follows: Vcc on pin 10 and 20; ground on pins 1, 2, 11 and 12; and – 12 VDC on pin 19. Capacitors C8 and C10 through C20 provide filtering.

SWITCH (FUNCTION)	POSITION ** (MDI VALUE)	ENCODER IC14 PIN (B)						PROM									
								SELECTION *		WORD OUTPUT PIN (Q)							
		S	PROM ADDRESS							HIGH ORDER				LOW ORDER			
		38 (2)	1 (3)	40 (4)	39 (9)	33 (5)	34 (6)	IC15	IC16	9 (7)	7 (6)	6 (5)	5 (4)	4 (3)	3 (2)	2 (1)	1 (1b)
S2 (FUNCTION)	RESTART	1	0	0	1	0	1	Z	S	1	1	1	0	0	0	0	0
	CONTINUE	0	1	1	0	1	1	S	Z	1	1	1	0	0	0	1	0
S7 (HOLD)	HOLD	1	0	1	1	1	0	Z	S	1	1	1	0	0	1	0	0
S10	XY/TI	1	0	0	1	0	0	Z	S	1	1	0	0	0	0	0	0
ABS/TLO	Z/TNO	0	1	1	0	1	0	S	Z	1	1	0	0	0	0	1	0
S9	+	0	1	0	0	0	0	S	Z	1	1	0	0	0	1	0	0
(AXIS MOTION)	−	0	0	0	1	1	0	S	Z	1	1	0	0	0	1	1	0
S8	EDIT	0	1	0	0	0	1	S	Z	1	1	0	0	1	0	1	0
(FUNCTION)	RDI	0	0	0	1	1	1	S	Z	1	1	0	0	1	1	0	0
MDI (KEYBOARD)	Ø	0	1	0	1	0	1	S	Z	0	0	0	0	0	0	0	0
	1	0	0	1	0	1	0	S	Z	0	0	0	0	0	0	0	1
	2	0	0	0	0	1	0	S	Z	0	0	0	0	0	0	1	0
	3	0	0	0	0	0	0	S	Z	0	0	0	0	0	0	1	1
	4	0	0	1	1	0	0	S	Z	0	0	0	0	0	1	0	0
	5	0	0	0	1	0	0	S	Z	0	0	0	0	0	1	0	1
	6	0	0	0	0	0	1	S	Z	0	0	0	0	0	1	1	0
	7	0	1	1	1	1	1	S	Z	0	0	0	0	0	1	1	1
	8	1	0	0	0	0	1	Z	S	0	0	0	0	1	0	0	0
	9	0	1	0	1	0	0	S	Z	0	0	0	0	1	0	0	1
	CE	0	1	1	0	0	0	S	Z	1	0	1	0	0	0	0	0
	N	1	0	0	0	0	0	Z	S	0	0	1	0	0	0	0	0
	G	0	1	0	1	1	1	S	Z	0	0	1	0	0	0	0	1
	F	0	1	0	1	1	0	S	Z	0	0	1	0	0	0	1	0
	M	0	1	1	1	1	0	S	Z	0	0	1	0	0	0	1	1
	X	0	0	1	1	1	0	S	Z	0	0	1	0	0	1	0	0
	Y	0	0	1	0	1	1	S	Z	0	0	1	0	0	1	0	1
	Z	0	0	0	0	1	1	S	Z	0	0	1	0	0	1	1	0
	− =	0	0	1	1	0	1	S	Z	0	1	0	0	0	0	0	0
	EOB(BLACK)	1	0	0	0	1	0	Z	S	0	1	1	0	0	0	0	0

* S = SELECT BIT, SELECTED PROM
Z = HIGH IMPEDANCE (NOT SELECTED)

** ALL SWITCH POSITIONS ARE DEPRESSED

Table 4-2 Encoder and PROM Output

MULTIPLEXING SIGNALS						SWITCH SELECTION			ADDRESS
K3-14 FKYSL	K3-16 FAL2L	K3-15	IC10 2	IC10 12	IC10 10	IC7, IC8, IC9	IC11	IC12	
H	H	H	L	L	L	S1 (MODE)	IRRELEVANT	S1	167460
H	H	L	L	L	H	S5 (ABS / TLO)	IRRELEVANT	S5	167462
H	L	H	L	H	L	S4 (AXIS MOTION)	IRRELEVANT	S4	167464
H	L	L	L	H	H	S3 (AXIS)	IRRELEVANT	S3	167466
L	H	H	H	L	L	IRRELEVANT	LOW ORDER BITS (SWITCH VALUE)	LOW ORDER BITS (SWITCH VALUE)	167470
L	H	L	H	L	H	IRRELEVANT	HIGH ORDER BITS (SWITCH FUNCTION)	HIGH ORDER BITS (SWITCH FUNCTION)	167472

Table 4-3 UFP Switch Multiplex Selection

Display Multiplex—Drawing 1040223, Sheet 1 is a detailed logic diagram of the UFP display function. The displays are visible through windows in the Operator's Main Control Panel. The displays consist of two types: discrete LED indicators and seven segment decimal readout LEDs.

Each type of display requires its own data. The discrete LEDs receive status data on four lines (INDbO through INDb3), and the seven segment decimal readouts receive BCD data on four lines (DBCDO through DCBD3).

On the ZDI board a 1KHz oscillator drives a 3-bit binary counter which counts continuously to generate signals DCNTRO through DCNTR. These signals are fed to the UFP board. On the UFP, IC1 decodes them to yield eight separate outputs (Zero, One, Two, Three, etc.) which pass through drivers and emerge as INDXO through INDX7. Each of these enables one digit of the numeric display and up to four Status LEDs. During the 2mS assigned to each set, the data for that set appears on the data inputs, INDbO through INDb3 for the Status LEDs and DBCDO through DBCD3 for the numeric displays. INDbO through INDb3 go through drivers IC5 and IC6 to the LEDs. The BCD data goes to the BCD-to-seven-segment decoder/driver IC4, whose outputs feed the seven segments of the numeric displays.

Drawing 1040223, sheet 1, includes a chart at the lower left that summarizes the operation of the Status LED indicator circuit. The numbers down the left side (167604 through 167616) identify the registers for the LEDs and the numbers across the top (INDbO through INDb3) identify the bits within the registers which apply to the individual LEDs. For example, if INDX3 is true during bit time INDbO (equivalent to setting the contents of address 167610 to a one) the inch decimal point will light.

4.2.3 UFP Address Listing

The following tables show the addresses of the LED registers, the numeric readouts and the display code. The status LEDs are write-only registers.

STATUS LEDS

Address	Contents	Function
167604	1	TLO LED
167604	2	Z LED
167604	4	Y LED
167604	10	X LED
167606	1	T LED
167606	2	S LED
167606	4	F LED
167606	10	N LED
167610	1	INCH D.P.
167610	2	DIA LED
167610	4	MINUS SGN
167610	10	HALF-STEP
167612	1	MM D.P.
167612	2	ABS LED
167612	4	TOOL LED
167612	10	CYCLE LED
167614	1	RDI LED
167614	2	ERR LED
167614	4	EDIT LED
167614	10	METRIC LED
167616	1	RUN LED
167616	2	GOTO LED
167616	4	HOLD LED
167616	10	WAIT LED

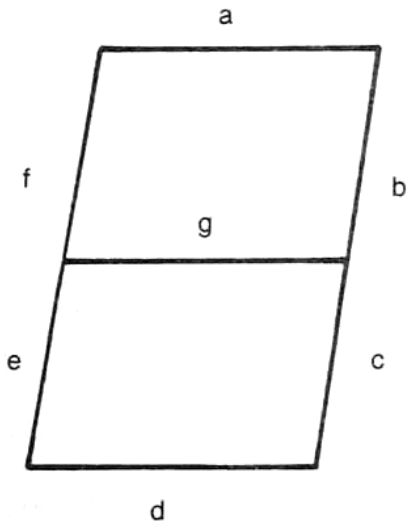
The numeric readouts are as follows:

ADDRESS	SEVEN-SEGMENT
167620	LED-1
167622	LED-2H
167624	LED-2L
167626	LED-3
167630	LED-4H
167632	LED-4L
167634	LED-5H
167636	LED-5L

The display conforms to the following code:

INPUT	DISPLAY	SEGMENTS
0	0	a,b,c,d,e,f
1	1	b,c
2	2	a,b,d,e,g
3	3	a,b,c,d,g
4	4	b,c,f,g
5	5	a,c,d,f,g
6	6	a,c,d,e,f,g
7	7	a,b,c
10	8	a,b,c,d,e,f,g
11	9	a,b,c,d,f,g
12		d,e,g
13		c,d,g
14		b,f,g
15		a,d,f,g
16		d,e,f,g
17	BLANK	NONE

The segment letters are those of a standard seven segment display:



The table shows the functions of the switch registers.

Sustained-action switches:

SWITCH	ADDRESS	CONTENTS	FUNCTION
MODE	167460	0	MDI STO
		2	MDI
		4	AUTO
		6	BLOCK
		10	SETUP
ABS/TLO	167462	0	ZERO
		2	GOTO
		4	TNO
		6	STORE
		10	GET
SET UP MOVE	167464	0	JOG
		2	1
		4	.1
		6	.01
		10	STEP
AXD SELECT	167466	0	X
		2	Y
		4	Z

Momentary-action switches, address 167472:

CONTENTS	FUNCTION
0	NUMERIC KEY
2	ALPHA KEY
4	— KEY
6	BLACK KEY (EOB)
12	CE KEY
14	SETUP
16	RESTART, START OR HOLD

4.3 ZDI LOGIC BOARD—Drawing 1040274

4.3.1 Interfacing Function

The ZDI board is an interface between external devices and the rest of the system. It is the primary communication between the LSI-11 and the paper tape reader, the Operator's Main Control Panel board (UFP), machine status switches, Operator's Local Panel switches, the axis drive board (SMD) and spindle control system. It communicates via the bus with the LSI-11 and the other logic boards in the system. We will describe the board by function as follows:

1. Bus drivers and receivers
2. Address decoding circuits
3. Readout display interface
4. External switch interface
5. Interrupt circuits
6. Tape reader interface
7. Control registers
8. External function drivers

4.3.2 Bus Interface

Bus Drivers and Receivers—Drawing 1040274, Sheet 1—The bus drivers and receivers consist of four chips, IC79 through IC82, each one with four separate driver/receiver pairs for a total of sixteen pairs. These

pairs are connected to the sixteen bus data/address lines, BDALOL through BDAL15L. Signals fed to the bus are identified as INOH through IN7H (the ZDI feeds no higher order bits to the bus), while signals received from the bus are identified as BRDOH through BRD15H.

Logic levels on control pins 7 and 9 of the four chips determine whether the driver/receiver pairs function as drivers or receivers. With a low level on both pins, they function as drivers; otherwise they function as receivers. IC80 and IC79 are wired to receive only. These two chips monitor bus lines BDAL8L through BDAL15L and transfer them as BRD8H through BRD15H to the ZDI address decoding circuits.

Address Decoding Circuits—Drawing 1040274, Sheet 1— All ZDI addresses are in the range of 167XXX. Address decoder IC65 continuously monitors bits BRD9H through BRD12H and BBS7. When 167XXX appears pin 9 of the decoder goes high. During any bus transaction BSYNCL is asserted. This raises pin 7 of the decoder high, latching the decoder in its state at that moment. BSYNC also strobes IC66 and IC67. The chips then latch the 8 lowest address bits as ALO through AL7 (AL standing for Address Latched).

The ZDI board contains three kinds of registers: those which solely place data on the system bus, called read-only registers; those which only accept data from the bus, called write-only registers; and those which do both. Drawing 1040274, sheet 1, shows the logic circuits necessary to decode the addresses and functions given in Table 4-4.

Signals FAL1L, FAL2L and FKYSL, on K10, decode the External Switch Data Registers 167460 to 167476. The switch settings determine the contents of these registers and the computer reads then when the appropriate address is detected.

The Status Registers 167000 through 167376 are also fully decoded. They contain program flags which are set (or reset) when the appropriate addresses are detected.

The remaining addresses shown in Table 4-4 represent signals only partially decoded by the circuits in Drawing 1040274, sheet 1. These signals feed other circuits, shown in sheets 2 through 5, where the full addresses are ultimately decoded.

TABLE 4-4
ADDRESS DECODING LOGIC OF DRAWING 1040274 SHEET 1

DECODED ADDRESS	FUNCTION	DECODING LOGIC FIG 1040274
167600 DINL	READ-ONLY	IC70-3 IC70-6 IC69-6
167600 DOUTL	WRITE-ONLY	IC70-11 IC70-8 IC69-8
A400 RDL A420 RDL A440 RDL	READ-ONLY	IC71 IC70-6 IC69-6
A460 RDL A400 WRL A420 WRL A440 WRL A460 WRL	WRITE-ONLY	IC71 IC70-8 IC69-8 IC69-8
167460	MODE	IC41-2
167462	ABS/TLO	IC41-4
167464	AXIS MOTION	IC41-12
167466	AXIS SELECTION	IC77-6
167470	MDI	IC74-6
167472	MDI	IC69-11
167474	EXT. REQ.	IC59-6
167476	EXT. REQ.	IC71-4
	(EXTERNAL	IC70-6
	SWITCH	IC69-6
	DATA	IC42-3
	REGISTERS)	IC42-6
	READ-ONLY	IC42-11
167000		IC68
	STATUS	IC69-3
TO	REGISTERS	IC59-12
	READ/WRITE	IC50-11
167376		IC50-3 IC83-12

4.3.3 Readout Display Interface—
Drawing 1040274, Sheet 2

Drawing 1040274, sheet 2, shows the circuits that decode addresses 167600 through 167636. These contain machine status information. Sheet 2 also shows the logic used to update and multiplex this information for display in the Operator's Main Control Panel.

When signal 167600DINL from IC70-3 is low, IC44-6 decodes read-enable signal 16761X. When 167600DOUTL from IC70-11 is low, IC44 decodes write-enable signals 16760X through 16763X, on pins 9 through 12 respectively. In both cases, AL4H from IC67-7 and AL3H from IC66-7 select the signal decoded.

Write-enable signals, 16760X, 16761X, 16762X and 16763X, allow four register files, IC2, IC3, IC27 and IC28 respectively, to accept data from bus receiver/driver IC82. The data are written into locations determined by signals AL2H, from IC67-5, and AL1H, from IC66-2. These two signals decode the remaining octal digit of the data address.

Each register contains four word locations with four bits per word. The four registers thus occupy sixteen word locations as follows:

REGISTER FILE	LOCATION
IC2	167600 through 167606
IC3	167610 thorugh 167616
IC27	167620 through 167626
IC28	167630 through 167636

Signals DCNTROH, DCNTR1H, DCNTR2H and DCNTR2L read the data from these locations. Binary counter IC43 produces the first three signals. The last signal is DCNTR2H inverted by IC59-2. VCO IC58-8 drives the counter at a 1KHz ± 30 Hz rate. The counter cycles continuously from 0 through 7. During the first

four counts, while DCNTR2H is low and DCNTR2L is high, the counter extracts the data previously written into the four locations of each IC2 and IC27. During the next four counts, while DCNTR2H is high and DCNTR2L is low, the counter extracts the data from the four locations in each IC3 and IC28 register file.

The three counter signals are transferred to the UFP board through IC26 and K4. The data extracted from the four register files are also transferred to the UFP through K4. The UFP uses the counter signals to display the data in the Operator's Main Control Panel in the same sequence as the data are extracted from the register files.

An additional register file, IC1 in the ZDI board, handles the same data and occupies the same locations, 167610 through 167616, as IC3. IC3, however, transfers data from the system bus to the UFP board while IC1 accepts data from the bus, saves them and returns them to the bus. This is done to prevent data losses during display time.

4.3.4 External Switch Interface—Drawing 1040274, Sheet 3

Figure 4-5, extracted from Drawing 1040274, sheet 3, is a simplified block diagram of the external switch interface circuits. These circuits select and route data from manual and automatic switches to different address locations. The external switch interface operates under control of a counter circuit and the address decode logic.

The manual switches, located on the Operator's Main Control Panel and on the Special Operations Panel, consist of fixed position selectors, momentary action pushbuttons and combinations of both. These interface with the ZDI board through K10.

The automatic switches are located in the quill housing and at the travel limits of the X, Y and Z axes. They provide safety for the operator and machine and sensing for axes stop. The automatic switches interface with the ZDI through K5.

The UFP board multiplexes the Main Control Panel switch data into six lines. Four of these lines, FRD1H through FRD4H, contain switch status information; the other two, FDRDY and FJGSWH, contain information from momentary action switches. FRD1H through FRD4H transfer data through K10 directly to selector driver IC24. FDRDYH is an interrupt signal which occurs when any pushbutton switch is depressed. This signal is a high pulse and goes through interrupt circuits to the selector and debounce logic. FJGSWH occurs only when the Jog switch is pressed. This is a high signal and goes directly to the selector and debounce logic.

K7 has provisions for eight inputs but uses only five in this application. These five inputs come from the Special Operations Panel switches. Two inputs, SLDESW and OPSTSW, from the BLOCK DELETE Switch and the OPSTOP Switch, go the selector EC13. The remaining three, LDPPSW, CLRSW and RESSW from LOAD Switch and CLEAR/RESET Switch, go to the selector and debounce logic.

Although K5 and the optocouplers can handle twelve inputs, they handle only four in this application. These four inputs come from the automatic switches. Two outputs from the optocouplers, QDECSW and QUPSW, go to selector IC51. The other two, SPNLKS and AXLSW, go to the selector and debounce logic. QUPSW also goes through K1-L to the NTP board.

The selector and debounce logic, under controlled by a counter circuit, produces nine data and two control output signals. Part of the data go to selectors IC13, IC51, part go to latch IC54, and the rest go to both selectors and latch circuits. One of the control signals, STROBE, goes to the interrupt logic and the other, RESSWL, goes through an open collector driver to the system bus. This signal emerges from the ZDI through K2-18 as BDCOK. RESSWL also goes directly from the selector and debounce logic to the external function drivers.

IC13 and IC51 form a sixteen line to two line selector. The two outputs, selected by the address decode logic, go through IC50 to set (or reset) flags BDALO and BDAL15.

The six output signals from latch IC54 go to selectors IC24 and IC25. These selectors, under control from the address decode logic, transfer data from either IC54 or from K10 to bus receiver/driver IC82. This receiver/driver transmits the selected data directly to the system bus.

4.3.5 Interrupt Circuits—Drawing 1040274, Sheet 4

Figure 4-6 is taken from Drawing 1040274, sheet 4, and shows a detailed logic diagram of the ZDI board interrupt circuits. Figure 4-7 shows the same circuits in a simplified block diagram. These circuits assign priorities and process three kinds of interrupt requests as follows:

1. A software generated interrupt request is detected by IC78-8, processed by the internal interrupt circuits and assigned first priority by the gating circuits.
2. A hardware generated interrupt request is detected by the external switch interface logic (Figure 4-7), processed by the external interrupt circuits and assigned second priority by the gating circuits. This interrupt occurs by the closure of any momentary action switch including the MDI keyboard and the axis limit switches.
3. An interrupt request by a peripheral device is detected by IC83-2 and assigned last priority by the gating circuits.

The internal and the external interrupt circuits store the software and the hardware interrupt requests respectively. If more than one interrupt request occurs simultaneously, the gating circuits pass the requests in descending order of priority and, once the interrupt is passed, they clear the stored interrupt.

When either a software or hardware interrupt occurs, the gating circuits pull the bus interrupt request BIRQL signal low and, simultaneously, trigger encoder IC75 to generate a four bit code which identifies the appropriate interrupt. The encoder also pulls IC74-8 and IC76-2 low to produce the bus reply, BRPLY L signal. This signal is also produced by either 16776DINL or